

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re patent application of:
Tilke et al.

MMB Docket No. 1890-0061

Application No. 10/780,276

Filed: February 17, 2004

For: Semiconductor Structure with
Increased Breakdown Voltage and
Method for Producing the
Semiconductor Structure

Examiner: To be assigned

Group Art Unit: To be assigned

I hereby certify that this correspondence is being deposited
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Box 1450, Alexandria, VA 22313-1450 on

June 14, 2004

(Date of deposit)

James D. Wood

Name of person mailing Document for fee

Signature

June 14, 2004

Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicant hereby discloses the following references,
copies of which are enclosed, with the exception of the U.S. patent and published patent
application, regarding the above-identified patent application.

Patent References

U.S. Patent No.

5,121,185

US 2002/0158308 A1

Inventor

Tamba et al.

Huber et al.

Issue Date

June 9, 1992

Oct. 31, 2002

Foreign Application
DE 100 44 838 A1

Issue Date
April 4, 2002

Country
Germany

Articles

- 1) O, Kenneth K., and Brad W. Scharf, "Effects of Buried Layer Geometry on Characteristics of Double Polysilicon Bipolar Transistors," IEEE Electron Device Letters, Vol., 19, No. 5, © May 1998, (3 pages).

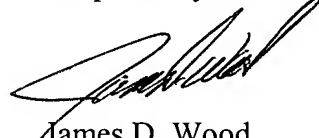
U.S. Patent Application Publication No. US 2002/0158308 A1 claims priority to DE 100 44 838 and may provide additional information.

Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed within three months after the filing date of the application or before the mailing of the first office action on the merits.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

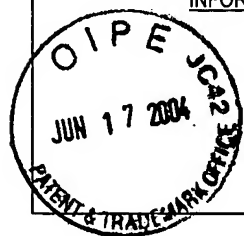
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Respectfully Submitted,



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FORM PTO-1449
INFORMATION DISCLOSURE STATEMENT



MMB DOCKET NO. 1890-0061

APPLICATION NO.: 10/780,276

APPLICANT(S): Tilke et al.

FILING DATE: February 17, 2004

GROUP ART UNIT: To be assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	5,121,185	June 9, 1992	Tamba et al.			
	AB	2002/0158308 A1	October 31, 2002	Huber et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	DE 100 44 838 A1	April 4, 2002	Germany			Yes No
	AM						Yes No
	AN						Yes No
	AO						Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	1	O, Kenneth K., and Brad W. Scharf, "Effects of Buried Layer Geometry on Characteristics of Double Polysilicon Bipolar Transistors," IEEE Electron Device Letters, Vol., 19, No. 5, © May 1998, (3 pages).
	AR	1	
	AS	1	

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.